What is claimed is:

1. A processor, having a plurality of instruction slots each of which stores an instruction to be executed in parallel, wherein one of the plurality of instruction slots is a first instruction slot and another one of the plurality of instruction slots is a second instruction slot, the processor being characterized by:

a special instruction stored in the first instruction slot being executed by a first functional unit that executes instructions stored in the first instruction slot and a second functional unit that executes instructions stored in the second instruction slot, while an instruction in the second instruction slot is executed by a third functional unit that executes instructions stored in the second instruction slot.

2. The processor of Claim 1, wherein:

the special instruction denotes addition and subtraction, and

one of the first and second functional units performs addition and the other subtraction, as denoted by the special instruction.

3. The processor of Claim 2, wherein the instruction is a multiply instruction, and the third functional unit is a multiplier.

4. A processor for executing a plurality of instructions in parallel, comprising:

an instruction register having at least first and second instruction slots, for storing the plurality of instructions;

first and second decoders, for respectively decoding the instructions stored in the first and second instruction slots;

first and second functional units, which, if a special instruction is decoded by the first decoder, together execute the special instruction under the control of the first decoder; and

a third functional unit, for executing an instruction in parallel with the execution of the special instruction, under the control of the second decoder.

5. The processor of Claim 4, wherein:

the special instruction denotes addition and subtraction, and

one of the first and second functional units performs

addition and the other subtraction, as denoted by the special instruction.

6. The processor of Claim 5, wherein the instruction is a multiply instruction, and the third functional unit is a multiplier.

7. A processor, for executing a plurality of instructions in parallel, comprising:

a first and second decoding means, each of which decodes instructions and generates decode results denoting the content of the instructions, wherein, if the first decoding means decodes a special instruction, the first decoding means generates a first-part decode result denoting a first-type calculation and a second-part decode result denoting a second-type calculation;

a first and second executing means, corresponding to each of the first and second decoding means, for executing instructions in parallel according to a decode result from the corresponding decoding means; and

a selecting means, for selecting the second-part decode result if the first decoding means decodes the special

instruction, and selecting the decode result from the second decoding means if the first decoding means decodes an instruction other than the special instruction,

wherein the second executing means includes:

a first functional unit, which executes instructions according to the decode result selected by the selecting means; and

a second functional unit, which executes instructions according to the decode result of the second decoding means,

and wherein, if the special instruction is decoded, the first executing means performs a first-type calculation, and, in the second executing means, the first functional unit performs a second-type calculation and the second functional unit executes an instruction other than a special instruction, decoded by the second decoding means.

8. The processor of Claim 7, wherein:

the special instruction includes an operation code denoting the first-type calculation and the second-type calculation, and first and second operands;

the first executing means performs the first-type calculation on the first and second operands, and stores a

calculation result in the first operand;

the second executing means performs the second-type calculation on the first and second operands, and stores a calculation result in the second operand.

9. The processor of Claim 8, wherein:

the first executing means includes an adder/subtracter;

the first functional unit is an adder/subtracter; and

the special instruction denotes addition as the first-type calculation and subtraction as the second-type calculation.

10. The processor of Claim 9, wherein the second functional unit is a multiplier and the instruction is a multiply instruction.

11. The processor of Claim 9, wherein the second functional unit is a data transfer unit and the instruction is a transfer instruction.

12. A processor that fetches long-word instructions, each comprising at least two instructions, from a program, and executes a plurality of instructions in parallel, wherein the

program includes special instructions for indicating a first-type calculation and a second-type calculation, the processor comprising:

an instruction register having first and second instruction slots, for storing each of the instructions in a long-word instruction;

a first decoding means, for decoding an instruction stored in the first slot, and if the instruction is a special instruction, generating a first decode result and a second decode result;

a first executing means, for executing an instruction in accordance with the first decode result;

a second decoding means, for decoding an instruction stored in the second slot and generating a third decode result in parallel with the decoding and generating performed by the first decoding means;

a selecting means, for selecting the second decode result if the special instruction is decoded by the first decoding means, and selecting the third decode result if an instruction other than a special instruction is decoded by the first decoding means; and

a second executing means, for executing an instruction

according to the decode result selected by the selecting means,

wherein the first executing means performs the first-type calculation if the special instruction is decoded by the first decoding means; and

the second executing means performs the second-type calculation if the second decode result is selected by the selecting means.

13. The processor of Claim 12, wherein:

the special instruction includes an operation code denoting the first-type calculation and the second-type calculation, and first and second operands;

the first executing means performs the first-type calculation on the first and second operands, and stores a calculation result in the destination indicated by the first operand;

the second executing means performs the second-type calculation on the first and second operands, and stores a calculation result in the destination indicated by the second operand.

14. The processor of Claim 13, wherein the second

executing means includes:

a first functional unit, which executes an instruction according to a decode result selected by the selecting means; and

a second functional unit, which executes an instruction according to the third decode result of the second decoding means,

wherein the first functional unit performs the second-type calculation according to the special instruction, and the second functional unit executes an instruction other than a special instruction in parallel with the special instruction according to the third decode result.

15. The processor of Claim 14, wherein:

the first executing means includes an adder/subtracter;

the first functional unit is an adder/subtracter; and

the special instruction denotes addition as the first-type calculation and subtraction as the second-type calculation.

16. The processor of Claim 15, wherein the second functional unit is a multiplier and the instruction is a multiply instruction.

17. The processor of Claim 15, wherein the second functional unit is a data transfer unit and the instruction is a transfer instruction.

18. A program conversion apparatus that changes a source program to an object program for a target processor executing long-word instructions, comprising:

a retrieving means, for retrieving a pair of instructions from the source program, the pair of instructions comprising a first instruction denoting a first-type calculation of two variables and a second instruction indicating a second-type calculation of the same two variables;

a generating means, for generating a special instruction corresponding to the retrieved pair, the special instruction comprising an operation code denoting the first-type calculation and the second-type calculation, and two operands representing the two variables,

an arranging means, for arranging the generated special instruction into a long-word instruction.

19. The program conversion apparatus of Claim 18, wherein

the first instruction denotes addition, and the second instruction denotes subtraction.

20. The program conversion apparatus of Claim 19, wherein:

the target processor includes a first instruction execution unit having a first calculation unit, and a second instruction execution unit having a second calculation unit and a multiplication unit, and

the arranging means retrieves a multiply instruction that does not share dependency with the special instruction generated by the generating means, and arranges the special instruction and the multiply instruction into one long-word instruction.